ADATA Technology Corp.

Memory Module Data Sheet

DDR4-2400(CL17) 260-pin SO-DIMM(W) 8GB Based on 8Gb Samsung B-Die

Version 1.0

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Revision History

Version	Changes	Page	Date
1.0	Formal release	-	2018/02/12

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General Description：

AD4I240038G17-BSSB is DDR4-2400(CL17)-17-17 SDRAM memory module. The SPD is programmed to JEDEC standard latency 2400Mbps timing of 17-17-17 at 1.2V. The module is composed of 8Gb CMOS DDR4 SDRAMs in FBGA package and one 4Kbit EEPROM in 8pin TDFN package on a 260pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 260 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features：

• Power supply (Normal)
  VDD & VDDQ = 1.2V ±0.06V
  VPP = 2.5V +0.25V / -0.125V
  VDDSPD = 2.25V to 3.6V
• 1.2V pseudo open-drain I/O
• Burst Length (BL):8 and 4 with Burst Chop(BC)
• Bi-directional, differential data strobe (DQS and /DQS)
• Differential clock input operation
• Write and Read leveling
• Double-data-rate architecture; two data transfers per clock cycle
• 16 internal banks; 4 groups of 4 banks each
• Internal self calibration through ZQ pin (RZQ:240 ohm±1%)
• Self refresh mode / Low-power auto refresh(LPASR) / Temperature controlled refresh(TCR)
• Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C
  - Commercial Temperature(0°C ~ 85 °C)
  - Industrial Temperature(-40°C ~ 95 °C)
• Tc of 0°C to 95°C
  64ms, 8192-cycle refresh at 0°C to 85°C / 32ms, 8192-cycle refresh at 85°C to 95°C
• 8-bit pre-fetch architecture
• On Die Termination, Nominal, Park, and Dynamic ODT
• Data bus inversion for data bus(DBI)
• Command / Address Parity
• Data bus Write CRC
• Lead-free and Halogen-free products are RoHS Compliant

Pin Assignment：

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	2	VSS	89	VSS	90	VSS	175	VSS	176	VSS
3	DQ5	4	DQ4	91	CB1, NC	92	CB0, NC	177	DQS4_c	178	DM4_n/DBI4_n, NC
5	VSS	6	VSS	93	VSS	94	VSS	179	DQS4_t	180	VSS
7	DQ1	8	DQ0	95	DQS8_c	96	DM8_n/DBI8_n, NC	181	VSS	182	DQ39
9	VSS	10	VSS	97	DQS8_t	98	VSS	183	DQ38	184	VSS
11	DQS0_c	12	DM0_n/DBI0_n, NC	99	VSS	100	CB6, NC	185	VSS	186	DQ35
13	DQS0_t	14	VSS	101	CB2, NC	102	VSS	187	DQ34	188	VSS
15	VSS	16	DQ6	103	VSS	104	CB7, NC	189	VSS	190	DQ45
17	DQ7	18	VSS	105	CB3, NC	106	VSS	191	DQ44	192	VSS
19	VSS	20	DQ2	107	VSS	108	RESET_n	193	VSS	194	DQ41
21	DQ3	22	VSS	109	CKE0	110	CKE1	195	DQ40	196	VSS
23	VSS	24	DQ12	111	VDD	112	VDD	197	VSS	198	DQS5_c
25	DQ13	26	VSS	113	BG1	114	ACT_n	199	DM5_n/DBI5_n, NC	200	DQS5_t
27	VSS	28	DQ8	115	BG0	116	ALERT_n	201	VSS	202	VSS
29	DQ9	30	VSS	117	VDD	118	VDD	203	DQ46	204	DQ47
31	VSS	32	DQS1_c	119	A12	120	A11	205	VSS	206	VSS
33	DM1_n/DBI1_n, NC	34	DQS1_t	121	A9	122	A7	207	DQ42	208	DQ43
35	VSS	36	VSS	123	VDD	124	VDD	209	VSS	210	VSS
37	DQ15	38	DQ14	125	A8	126	A5	211	DQ52	212	DQ53
39	VSS	40	VSS	127	A6	128	A4	213	VSS	214	VSS
41	DQ10	42	DQ11	129	VDD	130	VDD	215	DQ49	216	DQ48
43	VSS	44	VSS	131	A3	132	A2	217	VSS	218	VSS
45	DQ21	46	DQ20	133	A1	134	EVENT_n	219	DQS6_c	220	DM6_n/DBI6_n, NC
47	VSS	48	VSS	135	VDD	136	VDD	221	DQS6_t	222	VSS
49	DQ17	50	DQ16	137	CK0_t	138	CK1_t	223	VSS	224	DQ54
51	VSS	52	VSS	139	CK0_c	140	CK1_c	225	DQ55	226	VSS
53	DQS2_c	54	DM2_n/DBI2_n, NC	141	VDD	142	VDD	227	VSS	228	DQ50
55	DQS2_t	56	VSS	143	PARITY	144	A0	229	DQ51	230	VSS
57	VSS	58	DQ22	KEY		KEY		231	VSS	232	DQ60
59	DQ23	60	VSS	145	BA1	146	A10/AP	233	DQ61	234	VSS
61	VSS	62	DQ18	147	VDD	148	VDD	235	VSS	236	DQ57
63	DQ19	64	VSS	149	CS0_n	150	BA0	237	DQ56	238	VSS
65	VSS	66	DQ28	151	A14/WE_n	152	A16/RAS_n	239	VSS	240	DQS7_c
67	DQ29	68	VSS	153	VDD	154	VDD	241	DM7_n/DBI7_n, NC	242	DQS7_t
69	VSS	70	DQ24	155	ODT0	156	A15/CAS_n	243	VSS	244	VSS
71	DQ25	72	VSS	157	CS1_n	158	A13	245	DQ62	246	DQ63
73	VSS	74	DQS3_c	159	VDD	160	VDD	247	VSS	248	VSS
75	DM3_n/DBI3_n, NC	76	DQS3_t	161	ODT1	162	C0, CS2_n, NC	249	DQ58	250	DQ59
77	VSS	78	VSS	163	VDD	164	VREFCA	251	VSS	252	VSS
79	DQ30	80	DQ31	165	C1, CS3_n, NC	166	SA2	253	SCL	254	SDA
81	VSS	82	VSS	167	VSS	168	VSS	255	VDDSPD	256	SA0
83	DQ26	84	DQ27	169	DQ37	170	DQ36	257	VPP	258	VTT
85	VSS	86	VSS	171	VSS	172	VSS	259	VPP	260	SA1
87	CB5, NC	88	CB4, NC	173	DQ33	174	DQ32				

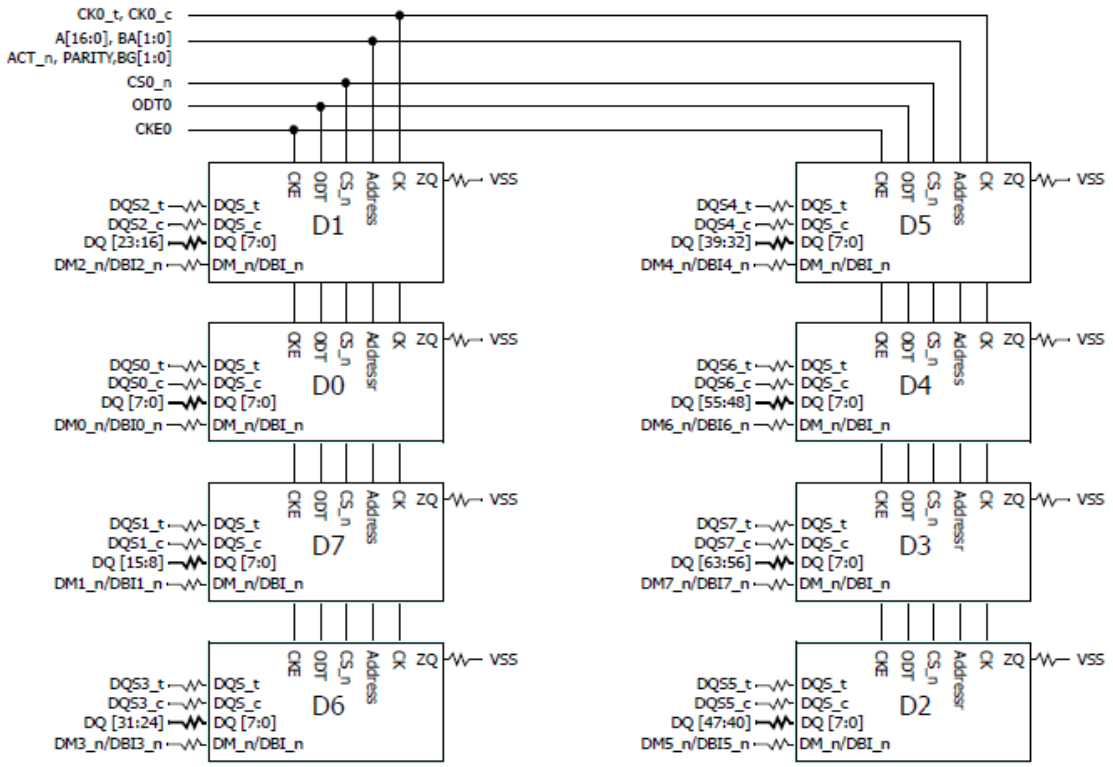
Pin Description：

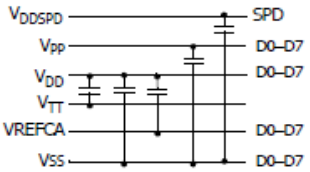
Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address bus	SCL	I2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n[4]	SDRAM write enable	12V	Optional power Supply on socket but not used on UDIMM`
CS0_n,CS1_n	DIMM Rank Select Lines	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	SDRAM on-die termination control lines	VDDSPD	Serial SPD/TSE positive power supply
ACT_n	SDRAM activate	ALERT_n	SDRAM ALERT_n
DQ0–DQ63	DIMM memory data bus	RESET_n	Set DRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS8_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS8_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)		
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)		
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

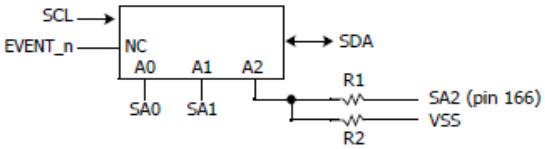
Block Diagram：

[8GB – 1Rank, 1024Mx8 DDR4 SDRAMs]





Serial PD with Thermal sensor



Note:

1. Unless otherwize noted, resistor values are 15Ω±5%.
2. ZQ resistors are 240Ω±1%.For all other resistor values refer to the appropriate wiring diagram.
3. To connect the SPD A2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The values for R1 and R2 are not critical. Any value less than 100 Ohms may be used.

Absolute Maximum Ratings：

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.5	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~1.5	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~3.0	V
Voltage on any pin relative to Vss	VIN, Vout	-0.3 ~ 1.5	V
Storage temperature	TSTG	-55 ~ +100	℃

Note: DDR4 SDRAM component specification.

Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	℃	
Extended Temperature Range (Optional)	TC	+85~+95	℃	1

Note: (1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 3.9μs

DC Operating Condition：

Voltage referenced to Vss = 0V, VDD&VDDQ=1.2V±0.06V, Tc = 0 to 85 ℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.14	1.2	1.26	V	1,2,3
	VDDSPD	2.25	2.5	3.6	V	
Supply Voltage for Output	VDDQ	1.14	1.2	1.26	V	1,2,3
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3
Reference Voltage for CMD/ADD	VREFCA, (DC)	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	4
Termination Voltage	VTT	0.49 x VDDQ-20mV	0.5 x VDD	0.51 x VDDQ+20mV	V	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.

(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

(3) The DC bandwidth is limited to 200MHz.

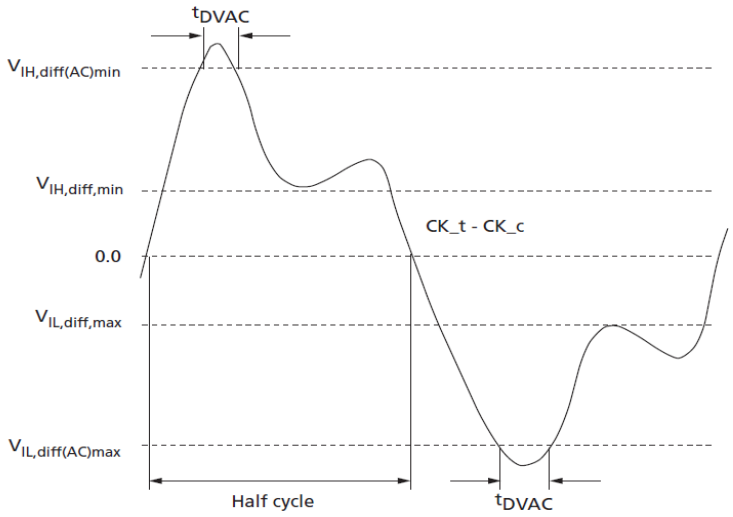
(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

Input DC & AC Logic Level for single-ended signals：

Parameter	Symbol	Min	Max	Unit	Note
DC Input logic high voltage	VIH.CA (DC75)	VREFCA+75	VDD	mV	
DC Input logic low voltage	VIL.CA (DC75)	VSS	VREFCA-75	mV	
AC input logic high	VIH.CA(AC100)	VREF+100	VDD	mV	1,2
AC input logic low	VIL.CA(AC100)	VSS	VREF–100	mV	1,2

Note: 1. See “Overshoot and Undershoot Specifications” on section.

2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)



Input AC &DC Logic Level for differential signals：

Parameter	Symbol	Min	Max	Unit	Note
Differential input high	VIHdiff	TBD	Note 3	V	1
Differential input low	VILdiff	Note 3	TBD	V	1
Differential input high AC	VIHdiff(AC)	2 (VIH(ac)-Vref)	Note 3	V	2
Differential input low AC	VILdiff (AC)	Note 3	2 x (VIL(ac)- Vref)	V	2

Notes: 1. Used to define a differential signal slew-rate.

2. For CK_t – CK_c use VIH/VIL(ac) of ADD/CMD and VREFCA

3. These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot on Component Datasheet.

IDD Specification：

VDDQ = VDD = 1.2V(1.14V~1.26V),PC4-19200

Symbol	Condition	8GB	Unit
IDD0[1]	One bank ACTIVATE-PRECHARGE current	296	mA
IPP0[1]	One bank ACTIVATE-PRECHARGE,wordline boost,IPP current	32	mA
IDD1[1]	One Bank Active-Read-Precharge Current	424	mA
IDD2N[2]	Precharge Standby Current	184	mA
IDD2NT[1]	Precharge standby ODT current	208	mA
IDD2P[2]	Precharge Power-Down Current	128	mA
IDD2Q[2]	Precharge Quiet Standby Current	168	mA
IDD3N[2]	Active standby current	288	mA
IPP3N[2]	Active standby IPP current	24	mA
IDD3P[2]	Active Power-Down Current	176	mA
IDD4R[1]	Burst Read Current	904	mA
IDD4W[1]	Burst write current	720	mA
IDD5B[1]	Burst refresh current (1x REF)	1776	mA
IPP5B[1]	Burst refresh IPP current (1x REF)	144	mA
IDD6N[2]	Self refresh current: Normal temperature range (0–85°C)	184	mA
IDD6E[2]	Self refresh current: Extended temperature range (0–95°C)	272	mA
IDD7[1]	Bank interleave read current	1384	mA
IPP7[1]	Bank interleave read IPP current	68	mA
IDD8[2]	Maximum power-down current	88	mA

Note:

1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N.

2. All ranks in this IDD/PP condition.

3.IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

Timings used for IDD, IPP and IDDQ Measurement：

Symbol		DDR4-1866	DDR4-2133	DDR4-2400	Units
Bin(CL-tRCD-tRP)		13-13-13	15-15-15	17-17-17	
Parameter		Min	Min	Min	
tCK		1.071	0.937	0.833	ns
CL		13	15	17	nCK
CWL		12	15	17	nCK
nRCD		13	15	17	nCK
nRC		45	51	56	nCK
nRAS		32	36	39	nCK
nRP		13	15	17	nCK
nFAW	X4	16	16	16	nCK
	X8	22	23	26	nCK
	X16	28	32	36	nCK
nRRDS	X4	4	4	4	nCK
	X8	4	4	4	nCK
	X16	5	6	7	nCK
nRRDL	X4	5	6	6	nCK
	X8	5	6	6	nCK
	X16	6	7	8	nCK
nRFC 2Gb		150	171	193	nCK
nRFC 4Gb		243	278	313	nCK
nRFC 8Gb		327	374	421	nCK
nRFC 16Gb		TBD	TBD	TBD	nCK

Timing Parameters:

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_total	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_total	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_total	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_total	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	125		107		94		83		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	63		54		47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$t_{ERR}(nper)min = ((1 + 0.68ln(n)) * t_{JIT}(per)\_total\ min)$ $t_{ERR}(nper)max = ((1 + 0.68ln(n)) * t_{JIT}(per)\_total\ max)$								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)	-	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)	-	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-		1,2,e, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.16	tCK(avg)/2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.76	-	tCK(avg)/2	13,17,18

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	16,17,18
Data Valid Window per device, per pin: tQH - tDQSQ each device's output	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	16,17,18
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	40
		NA	NA	NA	NA	NA	NA	1.8	NOTE44	tCK	41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
		NA	NA	NA	NA	NA	NA	1.8	NA	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		370		330		310		290	ps	37,38,39
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)		tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		txs(imin)		txs(imin)		txs(imin)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXS-DLL(min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIH-min	-	tISmin + tIH-min	-	tISmin + tIH-min	-	tISmin + tIH-min	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-RE_PAR	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD			
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE									ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34

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NOTE :

1. Start of internal write transaction is defined as follows : For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled

3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

5. WR in clock cycles as programmed in MR0.

6. tREFI depends on TOPER.

7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

12. The max values are system dependent.

13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.

14. The deterministic component of the total timing. Measurement method tbd.

15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.

16. This parameter will be characterized and guaranteed by design.

17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.

18. DRAM DBI mode is off.

19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI

23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge

24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge

25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.

26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.

27. This parameter has to be even number of clocks

28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).

32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).

33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

35. This parameter must keep consistency with Speed-Bin Tables shown in Device Operation.

36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2

37. applied when DRAM is in DLL ON mode.

38. Assume no jitter on input clock signals to the DRAM

39. Value is only valid for RZQ/7

40. 1tCK toggle mode with setting MR4:A11 to 0

41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400 speed grade.

42. 1tCK mode with setting MR4:A12 to 0

43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400 speed grade.

44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Device Operation. to Data Strobe Relationship". Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in See Device Operation Preamble".

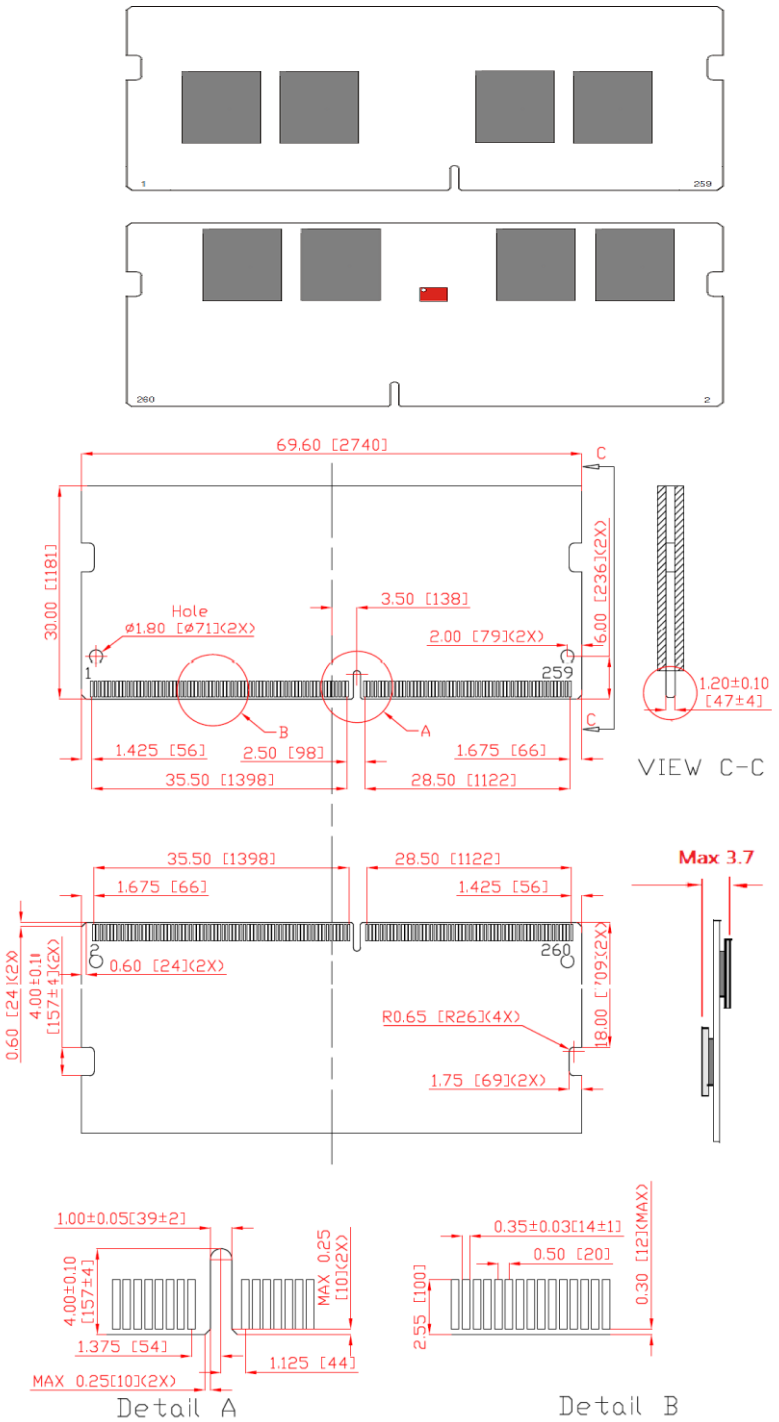
45.DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High

47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

Package Dimensions：

[8GB –1Rank, 1024Mx8 DDR4 SDRAMs]



Note: All dimensions are in millimeters(mils) and should be kept within a tolerance of ± 0.15(5.91),unless otherwise specified.

Ordering Information：

Server /IPC DRAM Module P/N Decoder

AD 4 I 2400 3 8G 17 - B SS B

BRAND
AD= ADATA

Module MODE
1= DDR
2= DDR2
3= DDR3
D= DDR3L
4= DDR4

MODULE TYPE

A=VLP SO-DIMM	M= Micro-DIMM
B= ECC SO-DIMM	R= R-DIMM
C= VLP ECC-DIMM	S= SO-DIMM
D= LR-DIMM	U= U-DIMM
E= ECC DIMM	V= VLP R-DIMM
F= FB-DIMM	X=VLP U-DIMM
I=SO-DIMM(W)	Y=VLP ECC SO-DIMM
L=LR-DIMM 1.5H	

SPEED

333= 333MHz	1066= 1066MHz
400= 400MHz	1333= 1333MHz
533= 533MHz	1600= 1600MHz
667= 667MHz	1866= 1866MHz
800= 800MHz	2133= 2133MHz
	2400= 2400MHz

COMPONENT CONFIG. CODE

A= 64x8	H=32x8	6=4Gbx4 (DDP)
B= 128x8	I=128x4	J=512x16
C= 256x8	V=2048x4	7=2048x8
D= 64x16	W=512x8	
E= 32x16	X=128x16	
F= 256x4	Y=1024x4	
G= 512x4	3=1024x8	

CAPACITY

128M= 128M	4G= 4G
256M= 256M	8G= 8G
512M= 512M	16G=16G
1G= 1G	32G=32G
2G= 2G	64G=64G

Die Version

A=A Die	M =M Die
B=B Die	E = E Die
C=C Die	N = N Die
D=D Die	Q = Q Die
F =F Die	P = P Die
G=G Die	
H=H Die	
J =J Die	
K=K Die	
Z=Don't Care (IPC/Server)	

Die Source
PF= PSC
NA= NANYA
HY=HYNIX
PR=PROMOS
EL=ELPIDA
MI=MICRON
SS=SAMSUNG
Z=Don't Care (IPC/Server)

PACKAGE CODE
B= Bulk
R= Retail
2= Dual-Kit Retail
3= Tri-Kit Retail
S= Single Tray
RM= Retail MAC
BUM= BULK+MAC HS

CAS LATENCY

2= CL2	7= CL7	15=CL15
25= CL2.5	8= CL8	17=CL17
3= CL3	9= CL9	
4= CL4	10=CL10	
5= CL5	11=CL11	
6= CL6	13=CL13	